



PCB LAYOUT GUIDE

JMB585 **PCIe Gen3x2 to SATA 6Gb/sx5 Bridge Controller**

Document No.: LOG-18001 / Revision: 1.3 / Date: 04/24/2019

JMicron Technology Corporation

1F, No. 13, Innovation Road 1, Science-Based Industrial Park,
Hsinchu, Taiwan 300, R.O.C.

Tel: 886-3-5797389

Fax: 886-3-5799566

Website: <http://www.jmicron.com>

Copyright © 2019, JMicon Technology Corp. All Rights Reserved.

Printed in Taiwan 2019

JMicron and the JMicon Logo are trademarks of JMicon Technology Corporation in Taiwan and/or other countries.

Other company, product and service names may be trademarks or service marks of others.

All information contained in this document is subject to change without notice. The products described in this document are NOT intended for use implantation or other life supports application where malfunction may result in injury or death to persons. The information contained in this document does not affect or change JMicon's product specification or warranties. Nothing in this document shall operate as an express or implied license or environments, and is presented as an illustration. The results obtained in other operating environments may vary.

THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROVIDED ON AN "AS IS" BASIS. In no event will JMicon be liable for damages arising directly or indirectly from any use of the information contained in this document.

For more information on JMicon products, please visit the JMicon web site at <http://www.JMicon.com> or send e-mail to sales@jmicon.com.

JMicron Technology Corporation

1F, No.13, Innovation Road 1, Science-Based Industrial Park, Hsinchu, Taiwan 300, R.O.C.

Tel: 886-3-5797389

Fax: 886-3-5799566

Revision History

Revision number	Effective date	Description of revision		Author
		Reference	Description of change	
1.0	02/14/2018	--	Initial release.	Jason Hsiao
1.1	04/09/2018	--	Modify PCIe trace description	Jason Hsiao
1.2	05/17/2018	--	1. Add PCIe trace mismatch description 2. Add power connect description	Jason Hsiao
1.3	04/24/2019	--	Add Impedance and Max trace length description	Jason Hsiao

Table of Contents

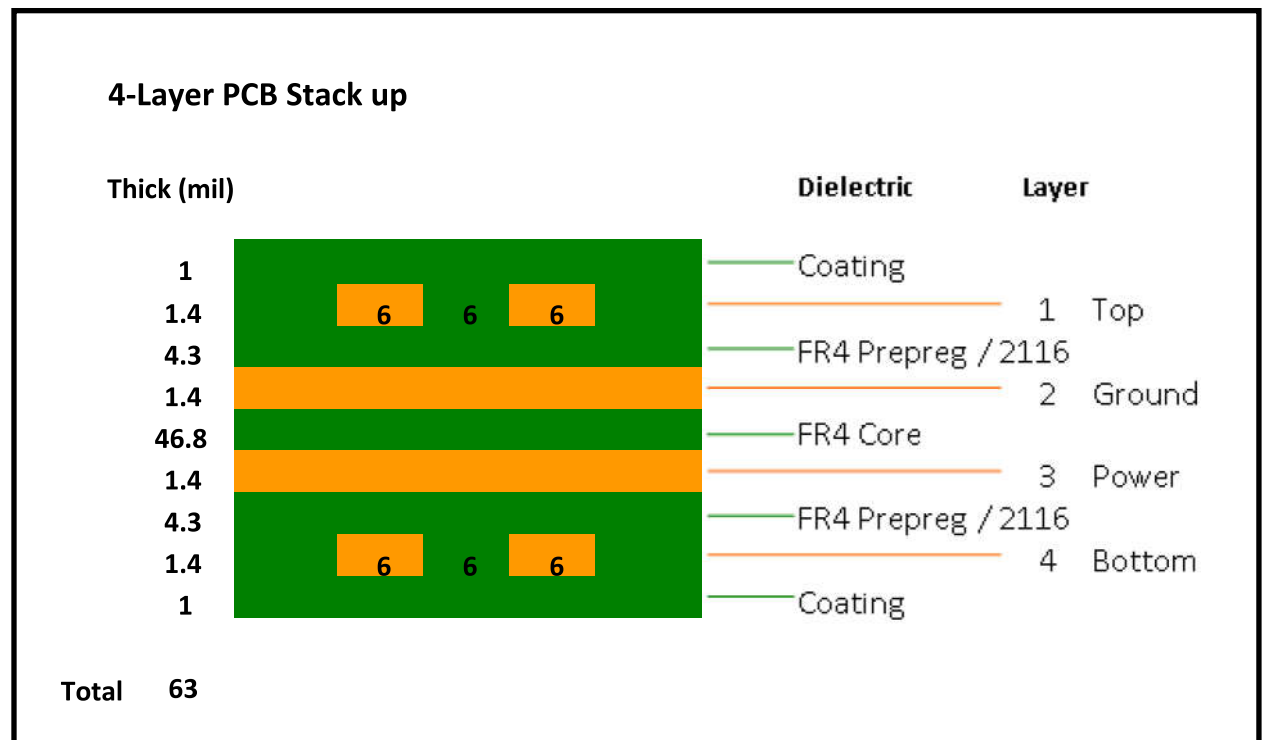
Revision History	ii
Table of Contents	iii
1 Overview	1
1.1 Description	1
1.2 PCB stack up	1
2 PCIe3.0 layout guide	2
2.1 Related net name & pairs.....	2
2.2 Net spacing & trace length rule	2
3 SATA3.0 layout guide	4
3.1 Related net name & pairs.....	4
3.2 Net spacing & trace length rule	4
4 Crystal layout guide	6
4.1 Related net name & pairs.....	6
4.2 Layout rule	6
5 Power layout guide	7
5.1 Related net name.....	7
5.2 Layout rule	7
6 PCIe and SATA layout example	8
6.1 PCIe interface	8
6.2 SATA interface.....	8

1 Overview

1.1 Description

This layout guide includes PCIe3.0, SATA3.0, Power plane, Crystal and Switching Regulator.

1.2 PCB stack up



2 PCIe3.0 layout guide

2.1 Related net name & pairs

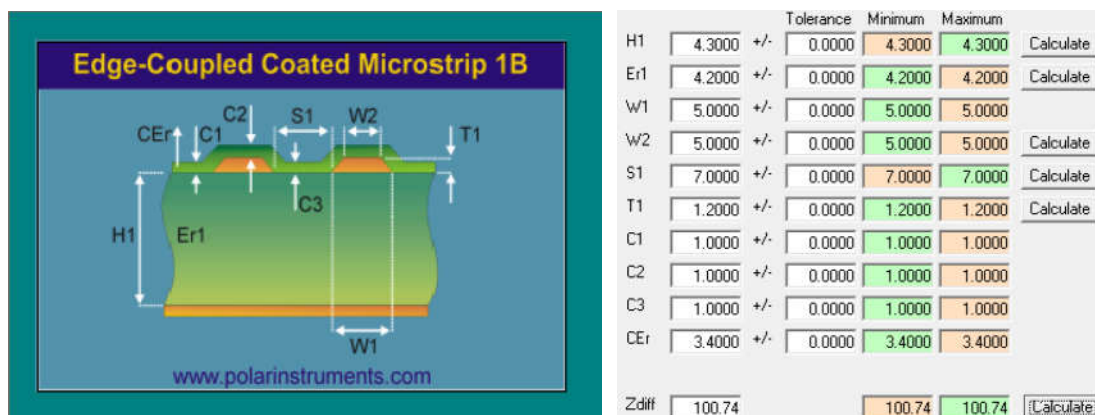
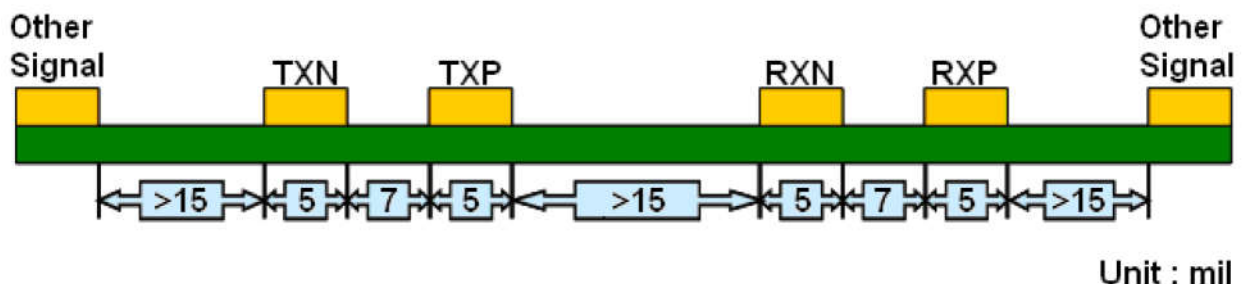
PCIe3.0 have 5 differential signal pair · detailed information is as follows:

Net name	Routing layer	Reference layer
P_TXP0, P_TXN0, P_RXN0, P_RXP0, P_TXP1, P_TXN1, P_RXN1, P_RXP1, P_CLKP, P_CLKN,	1st layer	2nd layer (GND)

2.2 Net spacing & trace length rule

- PCIe3.0 Impedance : 100 Ω + /-10 Ω
- PCIe3.0 Max Trace length to PCIe Host : 11 inch (27.94 cm)
- PCIe3.0 Trace : Trace Width / Trace Separation / Pair Separation = 5 / 7 / 15 mil]

Target differential impedance: 100 Ω



- P_TXP0, P_TXN0, P_TXP1, P_TXN1 trace length mismatch < 5mil.
- P_RXP0, P_RXN0, P_RXP1, P_RXN1 trace length mismatch < 5mil.

- P_CLKP, P_CLKN trace length mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.
- Route all PCIe signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Do not route PCIe traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

3 SATA3.0 layout guide

3.1 Related net name & pairs

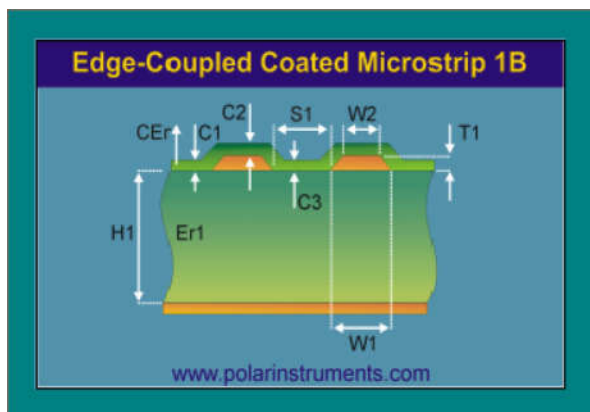
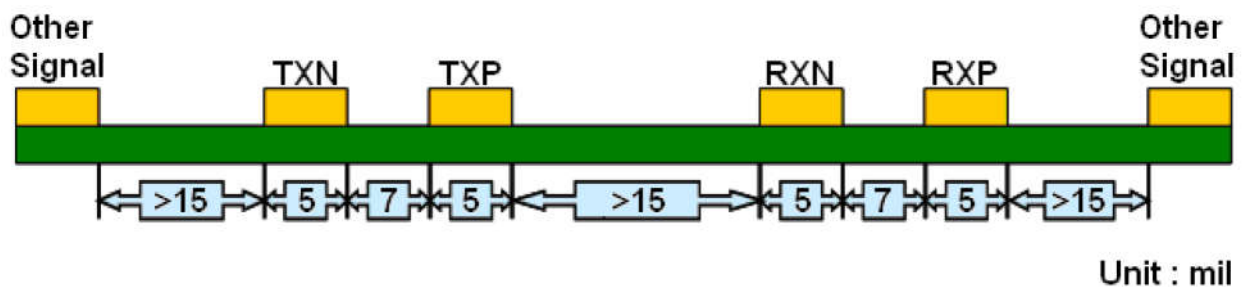
SATA3.0 have 10 differential signal pair , detailed information is as follows:

Net name	Routing layer	Reference layer
S_TXP0, S_TXN0, S_RXP0, S_RXN0, S_TXP1, S_TXN1, S_RXP1, S_RXN1, S_TXP2, S_TXN2, S_RXP2, S_RXN2, S_TXP3, S_TXN3, S_RXP3, S_RXN3, S_TXP4, S_TXN4, S_RXP4, S_RXN4	1st layer	2nd layer (GND)

3.2 Net spacing & trace length rule

- SATA3.0 Impedance : 100 Ω + /-10 Ω
- SATA3.0 Max Trace length to SATA Host : 10 inch (25.4 cm)
- SATA Trace : Trace width / trace separation / pair separation = 5 / 7 / 15 mil

Target differential impedance: 100 Ω



		Tolerance	Minimum	Maximum	
H1	4.3000 +/-	0.0000	4.3000	4.3000	Calculate
Er1	4.2000 +/-	0.0000	4.2000	4.2000	Calculate
W1	5.0000 +/-	0.0000	5.0000	5.0000	Calculate
W2	5.0000 +/-	0.0000	5.0000	5.0000	Calculate
S1	7.0000 +/-	0.0000	7.0000	7.0000	Calculate
T1	1.2000 +/-	0.0000	1.2000	1.2000	Calculate
C1	1.0000 +/-	0.0000	1.0000	1.0000	
C2	1.0000 +/-	0.0000	1.0000	1.0000	
C3	1.0000 +/-	0.0000	1.0000	1.0000	
CEr	3.4000 +/-	0.0000	3.4000	3.4000	
Zdiff	100.74		100.74	100.74	Calculate

- SATA3.0 trace length mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.

- Route all SATA signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Do not route SATA traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

4 Crystal layout guide

4.1 Related net name & pairs

The Oscillator/Crystal detailed information is as follows:

Net name	Routing layer	Reference layer
XIN, XOUT	1st layer	2nd layer (GND)

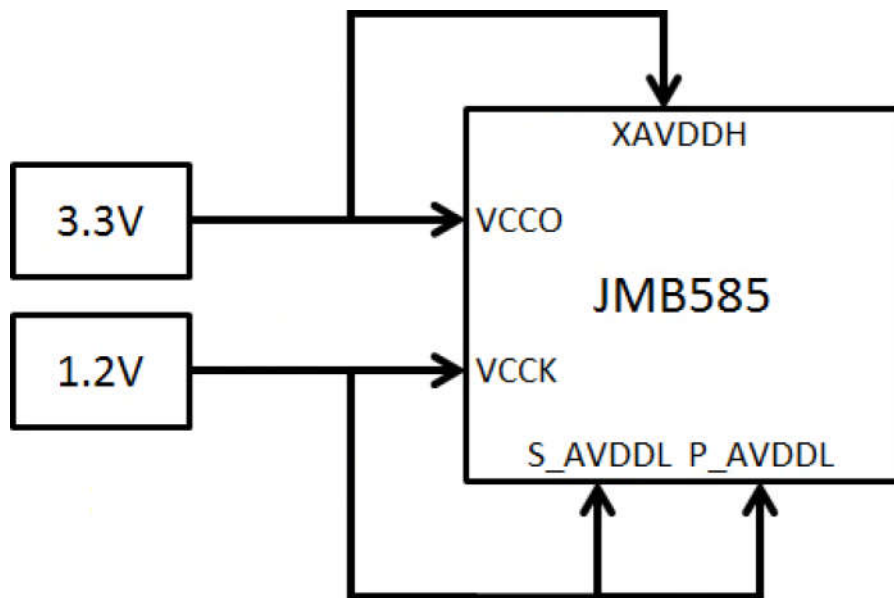
4.2 Layout rule

- The crystal unit should then be placed as close as possible to the XIN and XOUT pins to minimize etch lengths.
- Ensure that the ground plane under the IC and its components are of good quality.
- Avoid placing a separate ground under the oscillator and connecting it to the general ground through a single point.
- Avoid long connections to the crystal and to the load capacitor that create a large loop on the PCB.
- Use a short connection between the two crystal load capacitors and route the common connection to the IC ground reference.

5 Power layout guide

5.1 Related net name

Power detailed information is as follows:



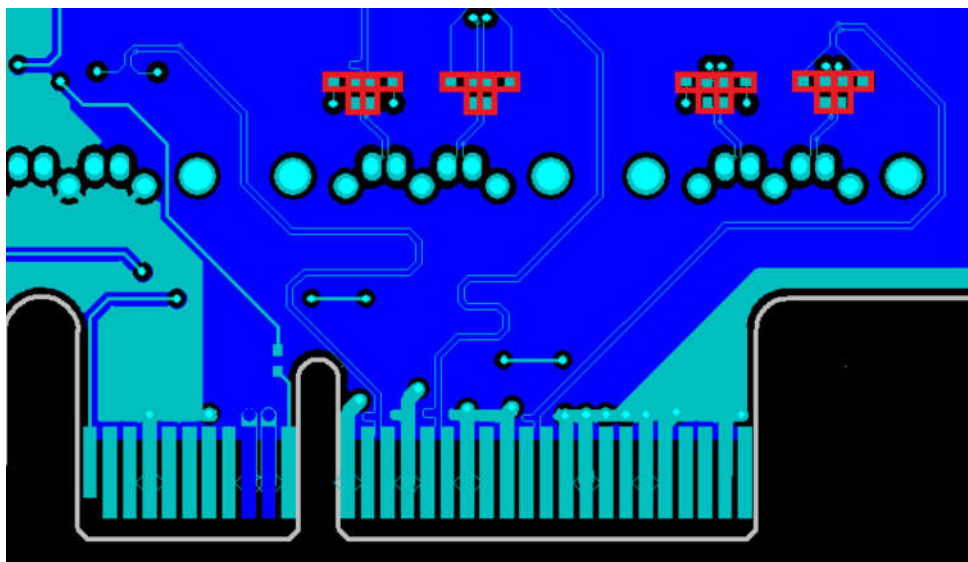
5.2 Layout rule

- The width of VCCO , XAVDDH $\geq$ 15 mil (suggest 30 mil), connect to VCCO first and then connect to XAVDDH
- The width of VCCK , P_AVDDL, S_AVDDL $\geq$ 50 mil (suggest 60 mil), connect to VCCK first and then connect to S_AVDDL, P_AVDDL

6 PCIe and SATA layout example

6.1 PCIe interface

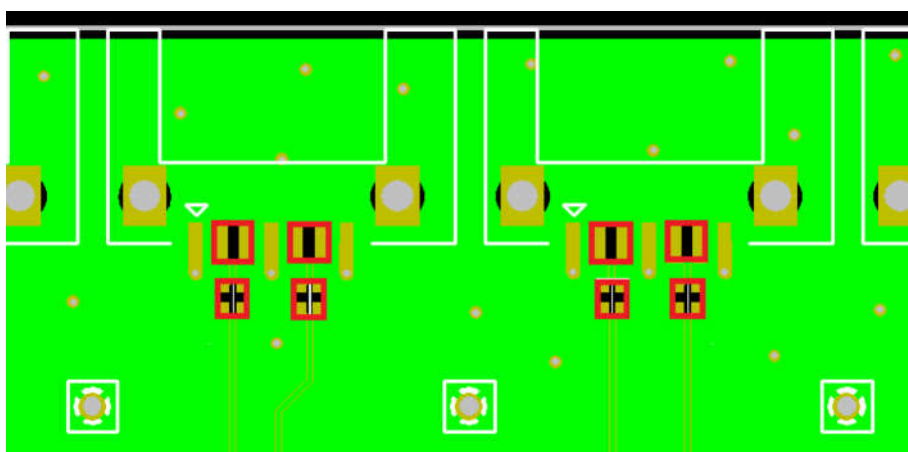
Layout example for PCIe connector:



Note: Remove area under capacitors

6.2 SATA interface

Layout example for SATA connector:



Note: Remove area under capacitors

<http://www.jmicron.com>



JMicron
Storing the World • Bridging the Future